In the Claims:

1. (Original) A method for arbitrating for access to a slave device, comprising:

initiating an access to the slave device by a master device;

determining that the access is an undefined length burst access, wherein the undefined length burst access comprises an undefined number of access beats;

determining that a predetermined number of access beats of the undefined length burst access will be transmitted between the master device and the slave device before allowing access to the slave device to be arbitrated;

determining that the predetermined number of access beats have occurred during the undefined length burst access; and

allowing arbitration for access to the slave device only after the predetermined number of access beats.

2. (Original) The method of claim 1 further comprising correlating the predetermined number of access beats to a value stored in a storage element of a data processing system.

3. (Original) The method of claim 1, further comprising providing a counter, and arbitrating for access to the slave device is allowed after each

time the counter counts the predetermined number of access beats.

4. (Original) The method of claim 1 further comprising arbitrating for access to the slave device on every access beat following the predetermined number of access beats during the undefined length burst access.

5. (Original) The method of claim 1, further comprising arbitrating for access to the slave device after the predetermined number of access beats in a modulus manner.

6. (Original) The method of claim 1, further comprising implementing the method in a data processing system having a plurality of master ports coupled to a plurality of slave ports via a crossbar switch.

7. (Original) An arbitration circuit for arbitrating access to a slave device by a plurality of master devices, the arbitration circuit comprising:

an undefined length burst arbitration circuit, coupled to the slave device and to the plurality of master devices, the undefined length burst arbitration circuit for determining that an access to the slave device is an undefined length burst access, and for allowing arbitration of the slave device only after a predetermined time period during the

undefined length burst access; and

a storage element for storing a value corresponding to the predetermined time period.

8. (Original) The arbitration circuit of claim 7, wherein the predetermined time period corresponds to a predetermined number of beats of the undefined length burst access.

9. (Original) The arbitration circuit of claim 8 further comprising a counter coupled to the storage element, the counter for counting the predetermined number of beats, the counter being reloaded after counting the predetermined number of access beats, and wherein arbitration for access to the slave device is allowed only after each time the counter counts the predetermined number of access beats during the undefined length burst access.

10. (Original) The arbitration circuit of claim 8 further comprising a counter coupled to the storage element, the counter for counting the predetermined number of beats, wherein arbitration for access to the slave device is allowed on every access beat following the predetermined number of access beats during the undefined length burst access.

11. (Original) The arbitration circuit of claim 7, wherein the predetermined time period corresponds to a predetermined number of system clock cycles.

12. (Original) The arbitration circuit of claim 11 further comprising a counter coupled to the storage element, the counter for counting the predetermined number of clock cycles, the counter being reloaded after counting the predetermined number of clock cycles, and wherein arbitration for access to the slave device is allowed only after each time the counter counts the predetermined number of clock cycles during the undefined length burst access.

13. (Original) The arbitration circuit of claim 11 further comprising a counter coupled to the storage element, the counter for counting the predetermined number of clock cycles, wherein arbitration for access to the slave device is allowed following the predetermined number of clock cycles during the undefined length burst access.

14. (Original) The arbitration circuit of claim 7, wherein the storage element is a bit field portion of a control register.

15. (Original) The arbitration circuit of claim 7, wherein the arbitration circuit is implemented in a data processing system having a plurality of slave devices coupled to the plurality of master devices via a crossbar switch.

16. (Original) A method for arbitrating for access to a slave device by a plurality of master devices, comprising:

initiating an access to the slave device by a master device of the plurality of master devices;

determining that the access is an undefined length burst access, wherein the undefined length burst access comprises an undefined number of access beats;

loading a counter with a first predetermined value;

changing a count value of the counter for each access beat until a second predetermined value is reached; and

allowing arbitration of access to the slave device to occur only after the count value is equal to the second predetermined value.

17. (Original) The method of claim 16, further comprising reloading the counter with the first predetermined value each time the counter reaches the second predetermined value.

18. (Original) The method of claim 16, further comprising reloading the counter with the first predetermined value after mastership of the slave device is lost.

19. (Original) The method of claim 16, further comprising implementing the method in a data processing system having a plurality of master ports coupled to a plurality of slave ports via a crossbar switch, one of the plurality of master ports being coupled to a corresponding master device of the plurality of master devices and the slave device coupled to one of the plurality of slave ports.

20. (Original) The method of claim 19, further comprising implementing the data processing system on an integrated circuit.